UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,857	03/31/2004	Robert E. Cypher	5681-13501	5571

58467 7590 03/25/2008

MHKKG/SUN
P.O. BOX 398
AUSTIN, TX 78767

EXAMINER	
ELAND, SHAWN	

ART UNIT	PAPER NUMBER
2188	

MAIL DATE	DELIVERY MODE
03/25/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/813,857
Filing Date: March 31, 2004
Appellant(s): CYPHER, ROBERT E.

Stephen Curran
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 01/21/08 appealing from the Office action mailed 07/09/07.

(1) Real Party in Interest

The appeal brief correctly names Sun Microsystems, Inc. as the assignee for application 10/813857.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,434,993	Liencres et a.	07-1995

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1 – 48 are rejected under **35 U.S.C. 102(b)** *as being anticipated by* ***Liencres*** *et al. (US PAT. 5,434,993).*

Claim 1

In regard to claim 1, Liencres teaches a plurality of nodes ***(see element 20 in figure 3a; see column 6, lines 13 – 15)*** coupled by an inter-node network ***(see element 31)***, wherein each node includes a plurality of active devices ***(see elements 21 & 35)***, a memory subsystem ***(see element 32)***, and an address network and a data network respectively configured to convey address packets and data packets between the plurality of active devices and the memory subsystem ***(see element 33)***; wherein a memory subsystem included in a node of the plurality of nodes is configured to maintain a response indication indicating whether the memory subsystem should send a data packet corresponding to a coherency unit in response to receiving from an

active device in the node an address packet requesting an access right to the coherency unit ***(see column 7, "Read Transactions")***; wherein the node is configured to store a node identifier for the coherency unit, wherein the node identifier identifies a different node of the plurality nodes in which the coherency unit is in a modified global access state ***(see column 7, lines 7 – 10; the status bits)***.

Claim 17

In regard to claim 17, Liencres teaches a plurality of client devices ***(see element 20 in figure 3a; see column 6, lines 13 – 15)*** including a memory subsystem ***(see element 32)***, an active device ***(see element 21)***, and an interface configured to send and receive coherency messages on an inter-node network coupling nodes in the multi-node computer system ***(see element 31)***; an address network configured to convey address packets between the plurality of client devices ***(see element 33)***; a data network configured to convey data packets between the plurality of client devices ***(see element 33)***; wherein the memory is configured to maintain a response indication indicating whether the memory should send a data packet corresponding to a coherency unit on the data network in response to receiving an address packet requesting an access right to the coherency unit from the active device ***(see column 7, "Read Transactions")***; wherein the node is configured to store a node identifier for the coherency unit, wherein the node identifier identifies a different node in the multi-node system in which the coherency unit is in a modified global access state ***(see column 7, lines 7 – 10; the status bits)***.

Claim 33

In regard to claim 33, Liencres teaches wherein the multi-node computer system includes a plurality of nodes coupled by an inter-node network ***(see elements 20 & 25 in figure 3a)***, wherein each node includes an active device ***(see element 21)***, a memory subsystem ***(see element 32)***, and an address network coupling the active device and the memory subsystem ***(see element 33)***, the method comprising: a memory subsystem included in a node of the plurality of nodes receiving from an active device included in the node an address packet requesting an access right to a coherency unit ***(see column 7, "Read Transactions")***; in response to said receiving, the memory subsystem sending a responsive data packet to the active device dependent on response indication associated with the coherency unit ***(see column 7, "Read Transactions")***; the node sending a coherency message requesting the access right to a different node of the plurality of nodes in response to a node identifier identifying the different node as a node in which the coherency unit is in a modified global access state ***(see column 7, "Read Transactions")***.

Claim 2

In regard to claim 2, Liencres teaches wherein each node includes an interface coupled to send and receive coherency messages on the inter-node network ***(see element 31)***, wherein an interface included in the node is configured to store the node identifier for the coherency unit ***(see column 7, lines 7 – 19)***.

Claim 18

In regard to claim 18, Liencres teaches wherein the interface is configured to store the node identifier for the coherency unit ***(see column 7, lines 7 – 10)***.

Claim 34

In regard to claim 34, Liencres teaches storing the node identifier for the coherency unit and sending the coherency message to the different node ***(see column 7, lines 7 – 19)***.

Claims 3, 19, & 35

In regard to claims 3 & 19, Liencres teaches wherein the interface is configured to store the node identifier in a global information cache that includes storage for a plurality of node identifiers for a plurality of coherency units ***(see element 46)***.

In regard to claim 35, Liencres teaches wherein said storing comprises the interface storing the node identifier in a global information cache that includes storage for a plurality of node identifiers for a plurality of coherency units ***(see element 46)***.

Claims 4, 20, & 36

In regard to claims 4 & 20, Liencres teaches wherein the interface included in the node is further configured to store a global access state of the coherency unit in the node ***(see column 7, lines 7 – 10; see column 1, lines 64 – 65)***.

In regard to claim 36, Liencres teaches the interface storing a global access state of the coherency unit in the node ***(see column 7, lines 7 – 10; see column 1, lines 64 – 65)***.

Claims 5, 21, & 37

In regard to claims 5 & 21, Liencres teaches wherein in response to receiving a coherency message sent by another one of the nodes requesting an access right to the coherency unit, the interface is configured to access the node identifier and to responsively send an additional coherency message to an interface included in the different node ***(see column 7, "Read Transactions")***.

In regard to claim 37, Liencres teaches in response to receiving a coherency message sent by another one of the nodes requesting an access right to the coherency unit, the interface sending an additional coherency message to an interface included in the different node identified by the node identifier ***(see column 7, "Read Transactions")***.

Claims 6, 22, & 38

In regard to claim 6, Liencres teaches wherein in response to receiving yet another coherency message acknowledging that the other one of the plurality of nodes gained the access right to the coherency unit, the interface included in the node is configured to update the node identifier to identify the other one of the plurality of nodes if an active device included in the other one of the plurality of nodes gained write access to the coherency unit ***(see column 7, "Write Transactions")***.

In regard to claim 22, Liencres teaches wherein in response to receiving yet another coherency message acknowledging that the other one of the plurality of nodes gained the access right to the coherency unit, the interface is configured to update the node identifier to identify the other one of the plurality of nodes if an active device included in the other one of the plurality of nodes gained write access to the coherency unit ***(see column 7, "Write Transactions")***.

In regard to claim 38, Liencres teaches in response to receiving yet another coherency message acknowledging that the other one of the plurality of nodes gained the access right to the coherency unit, the interface updating the node identifier to identify the other one of the plurality of nodes if an active device included in the other one of the plurality of nodes gained write access to the coherency unit ***(see column 7, "Write Transactions")***.

Claims 7, 23, & 39

In regard to claim 7, Liencres teaches wherein if the interface included in the node updates the node identifier, the interface is configured to send an address packet indicating a new value of the node identifier to the memory subsystem included in the node ***(see column 7, "Write Transactions"; see elements 34 & 46; see column 6, lines 64 – 67; see column 7, lines 7 – 10)***.

In regard to claim 23, Liencres teaches wherein if the interface updates the node identifier, the interface is configured to send an address packet indicating a new value of the node identifier to the memory subsystem ***(see column 7, "Write Transactions"; see elements 34 & 46; see column 6, lines 64 – 67; see column 7, lines 7 – 10)***.

In regard to claim 39, Liencres teaches the interface sending an address packet indicating a new value of the node identifier to the memory subsystem if the interface updates the node identifier ***(see column 7, "Write Transactions"; see elements 34 & 46; see column 6, lines 64 – 67; see column 7, lines 7 – 10)***.

Claims 8, 24, & 40

In regard to claims 8 & 24, Liencres teaches wherein the memory subsystem is configured to update the response indication in response to receiving address packets from one or more active devices included in the node ***(see column 8, lines 13 – 32)***.

In regard to claim 40, Liencres teaches the memory subsystem updating the response indication in response to receiving address packets from one or more active devices included in the node ***(see column 8, lines 13 – 32; the data is prepared for write-back)***.

Claims 9, 25, & 41

In regard to claims 9, 25, & 41, Liencres teaches updating the response indication to indicate that the memory subsystem should not respond to address packets requesting an access right to the coherency unit in response to receiving an address packet requesting a write access right to the coherency unit from one of the one or more active devices ***(see column 8, lines 33 – 46)***.

Claims 10, 26, & 42

In regard to claims 10, 26, & 42, Liencres teaches updating the response indication to indicate that the memory subsystem should respond to address packets requesting an access right to the coherency unit in response to receiving an address packet requesting to write a new value of the coherency unit to the memory subsystem ***(see column 8, lines 63 – 68; write-back should stop)***.

Claims 11, 27, & 43

In regard to claims 11, 27, & 43, Liencres teaches not updating the response indication in response to address packets requesting a shared access right to the coherency unit ***(see column 9, lines 1 – 8)***.

Claims 12, 28, & 44

In regard to claims 12, 28, & 44, Liencres teaches the memory subsystem sending a packet corresponding to the address packet to the interface if: the response indication indicates that the memory should not respond; the coherency unit is in a shared global access state in the node; and the address packet requests write access to the coherency unit ***(see column 8, lines 33 – 46)***.

Claims 13, 29, & 45

In regard to claims 13 & 29, Liencres teaches wherein in response to the packet corresponding to the address packet, the interface is configured to send a coherency message requesting write access to the coherency unit to the different node identified by the node identifier ***(see column 7, "Write Transactions")***.

In regard to claim 45, Liencres teaches the interface sending a coherency message requesting write access to the coherency unit to the different node identified by the node identifier in response to receiving the packet corresponding to the address packet ***(see column 7, "Write Transactions")***.

Claims 14, 30, & 46

In regard to claims 14, 30, & 46, Liencres teaches sending a packet corresponding to the address packet to the interface if: the response indication indicates that the memory should not respond; and the coherency unit is in an invalid global access state in the node ***(see column 8, lines 63 – 68)***.

Claims 15, 31, & 47

In regard to claim 15, Liencres teaches the node is configured to update the node identifier in response to receiving coherency messages from other ones of the plurality of nodes via the inter-node network ***(see column 7, "Write Transactions")***.

In regard to claims 31 & 47, Liencres teaches the node updating the node identifier in response to the interface receiving coherency messages from other nodes in the multi-node system ***(see column 7, "Write Transactions")***.

Claims 16, 32, & 48

In regard to claims 16, 32, & 48, Liencres teaches an active device that sends the address packet specifying the coherency unit gaining the access right to the coherency unit in response to receiving the data packet from the memory subsystem if the memory subsystem sends the data packet ***(see column 7, "Write Transactions")***.

(10) Response to Argument

Independent Claims

Appellant argues that the claim language limits the address network and data network to separate entities. The Examiner respectfully disagrees. The address and data networks are identified by the types of packets they transfer. The networks are not necessarily claimed as separate entities. The word "respectively" is used, but sending address packets and then data packets would fit the scope of the claims. One of the definitions of "respectively" is "each in the order given." Furthermore, the context of the claim could also be interpreted that "respectively" refers to the three elements – i.e. the active devices, the memory subsystem, and the address and data network – respectively conveying address and data packets. Compare this with, for example, the active devices, the memory subsystem, the address network, and the data network respectively conveying packets. The latter clearly delineates four separate elements. The claims, in their current form, respectfully do not.

Appellant argues that element 33 does not convey address packets between the active device and memory. The Examiner would like to point out in figure 3b that each bus cache controller must go through element 33 in order to use the active devices 21 & 35.

Appellant further argues that while the status bits may show if the current node is the owner, it does not infer that the status bits indicate the node that is the owner. The bits are set for "valid,"

"shared," and "owned." When the "valid" bit is not set (i.e. the current cache line is not valid) and the "shared" bit is marked, this identifies that another node now owns the data and is modifying it. (See the explanations for figure 1a - 1b in Liencres for further reference, if desired.) The Examiner would also like to further point out that the claim language does not necessarily imply true ownership of a coherency unit. It, in fact, discusses access rights which may be entirely separate from actual ownership (see [0092] in Specification; figures 10a & 10b in the Drawings). This makes the definition of node identifier vague.

Separately Argued Dependent Claims

This section is just a repeat of the status bits/ownership argument made in the arguments for the independent claims. The Examiner's response to this is the same as was given in the response to arguments section above but is posted below for convenience:

Appellant further argues that while the status bits may show if the current node is the owner, it does not infer that the status bits indicate the node that is the owner. The bits are set for "valid," "shared," and "owned." When the "valid" bit is not set (i.e. the current cache line is not valid) and the "shared" bit is marked, this identifies that another node now owns the data and is modifying it. (See the explanations for figure 1a - 1b in Liencres for further reference, if desired.) The Examiner would also like to further point out that the claim language does not necessarily imply true ownership of a coherency unit. It, in fact, discusses access rights which may be entirely separate from actual ownership (see [0092] in Specification; figures 10a & 10b in the Drawings). This makes the definition of node identifier vague.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Shawn Eland/

Examiner, Art Unit 2188

Conferees:

/Hyung S SOUGH/
Supervisory Patent Examiner, Art Unit 2188

/Manorama Padmanabhan/

Quality Assurance Specialist, TC2100, WG2180